REMARKS

Applicant submits the within amendment in response to the Official Action mailed August 28, 2002. A petition for a one-month extension of the term for response to said Official Action, to and including December 28, 2002, is transmitted herewith.

Applicant also submits herewith an Information Disclosure Statement pursuant to 37 C.F.R. § 1.97(e)(2).

In the Official Action, the drawings were objected to under 37 C.F.R. § 1.83(a) because the features specified in claims 5-8 must be shown. The drawings have been corrected to respond to this objection. Specifically, a new red-marked drawing showing a portion of a process flow chart with boxes labeled "apply gas under pressure" and "maintain gas pressure" has been enclosed as proposed new Fig. 9. The new drawing figure and specification description are supported by the originally filed claims 5-8 and by page 27, line 6 to page 27, line 26 of the originally filed specification. New, formal drawings incorporating the changes will be submitted upon Examiner's approval of the new Fig. 9. As such, the objection should be withdrawn.

Claims 1-3, 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Degani*, U.S. Patent 5,473,512. Applicant has amended claim 1 to respond to this rejection. Specifically, claim 1 has been amended to include the concept of placing the liquid on the top surface of the dielectric element at the edges of the chip and applying a gas under pressure around the chip and dielectric element to force the liquid into the spaces between the posts. *Degani* does not teach or suggest such a feature. *Degani* merely introduces a gel medium by inserting it in its uncured state through a localized cylindrical aperture while excess air is expelled through the

other aperture. (Col. 5, lns. 42-45.) Since *Degani* does not include the step of applying pressure around the chip and dielectric element to force the liquid into the spaces between the posts, the rejection should be withdrawn.

Claim 5 has been amended to reflect the amendment to claim 1 and, thereby, avoid any redundancies in claim 5.

Claims 9-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable on *Ishida et al.*, U.S. Patent 5,289,039 in view of *Burns et al.*, U.S. Patent 5,369,056. *Ishida* teaches an encapsulation process in which a metal heat radiating plate 7 is held above a wire-bonded IC 1 during an encapsulation molding operation. (Col. 4, lns. 24-34.) The Examiner acknowledges that "Ishida does not appear to explicitly teach the spreader (heat radiating plate) having a coefficient of thermal expansion substantially equal to the coefficient of thermal expansion of the chip." (Official Action at 8.) *Burns* teaches a process for modifying an already molded lead frame package (P, Fig. 3) by grinding off a portion of the encapsulant "to make the integrated circuit package thinner" (col. 3, lns. 15-17) and then mounting "a thin layer of material with a coefficient of thermal expansion that is equal to or less than the coefficient of thermal expansion of silicon" (col. 3, lns. 22-25), or as alternatively stated "with a coefficient of thermal expansion less than that of silicon" (col. 7, lns. 48-50) to the upper major surface of the integrated circuit package. The thin layer of material is selected to control bending moments in the package and prevent warping, while maintaining the thinnest package possible. (Col. 3, lns. 21-27.) The preferred material for layer 41 is Invar. (Col. 3, lns. 28-31.) There is no suggestion to combine *Burns* with *Ishida*, however. *Burns* suggests using the layer of low expansion material 41 only in the situation where one removes a part of the encapsulant in a lead frame package and only when a portion of the package is

removed by grinding after molding. (Col. 3, lns. 12-31.) Indeed, it is not clear from the references themselves whether mere substitution of *Burns'* low expansion layer for *Ishida's* metal layer would minimize or increase warping in a package as contemplated by *Ishida*, or whether such a substitution would be applicable in a wire-bonded package having some significant thickness above the front plane of the chip. As such, the two references in combination would not teach all the elements of claims 9 and 15.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: December 30, 2002

Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

IN THE CLAIMS

1. (AMENDED) A method of making a semiconductor chip assembly comprising the steps of:

(a) providing a dielectric element having top and bottom surfaces and terminals on said bottom surface;

(b) supporting semiconductor chip having a front surface with contacts thereon, a rear surface and edges extending between said front and rear surfaces above said top surface of said dielectric element by means of a plurality of posts extending between said rear surface of the chip and the top surface of the dielectric element; then

(c) applying a first curable liquid so that said first liquid penetrates between said rear surface and said top surface and penetrates between said posts wherein said step of applying said first liquid includes the steps of placing said first liquid on said top surface of said dielectric element at edges of said chip and applying pressure around the chip and dielectric element to thereby force said first liquid into the spaces between said posts; then

(d) curing said first liquid to form a flexible rear encapsulant;

(e) connecting said contacts to said terminals by connecting flexible leads between said contacts on said front surface and electrically conductive elements on said dielectric element; and

(f) providing a flexible lead encapsulant around said chip and said flexible leads.

5. (AMENDED) A method as claimed in claim 1 wherein said ~~step of applying said first liquid includes the steps of placing said first liquid on said top surface of said dielectric element at edges of said chip and applying a gas under pressure~~

~~around the chip and dielectric element to thereby force said first liquid into the spaces between said posts~~application of pressure around the chip and dielectric element is a gas under pressure.